MICROPROCESSORS AND MICROCONTROLLERS

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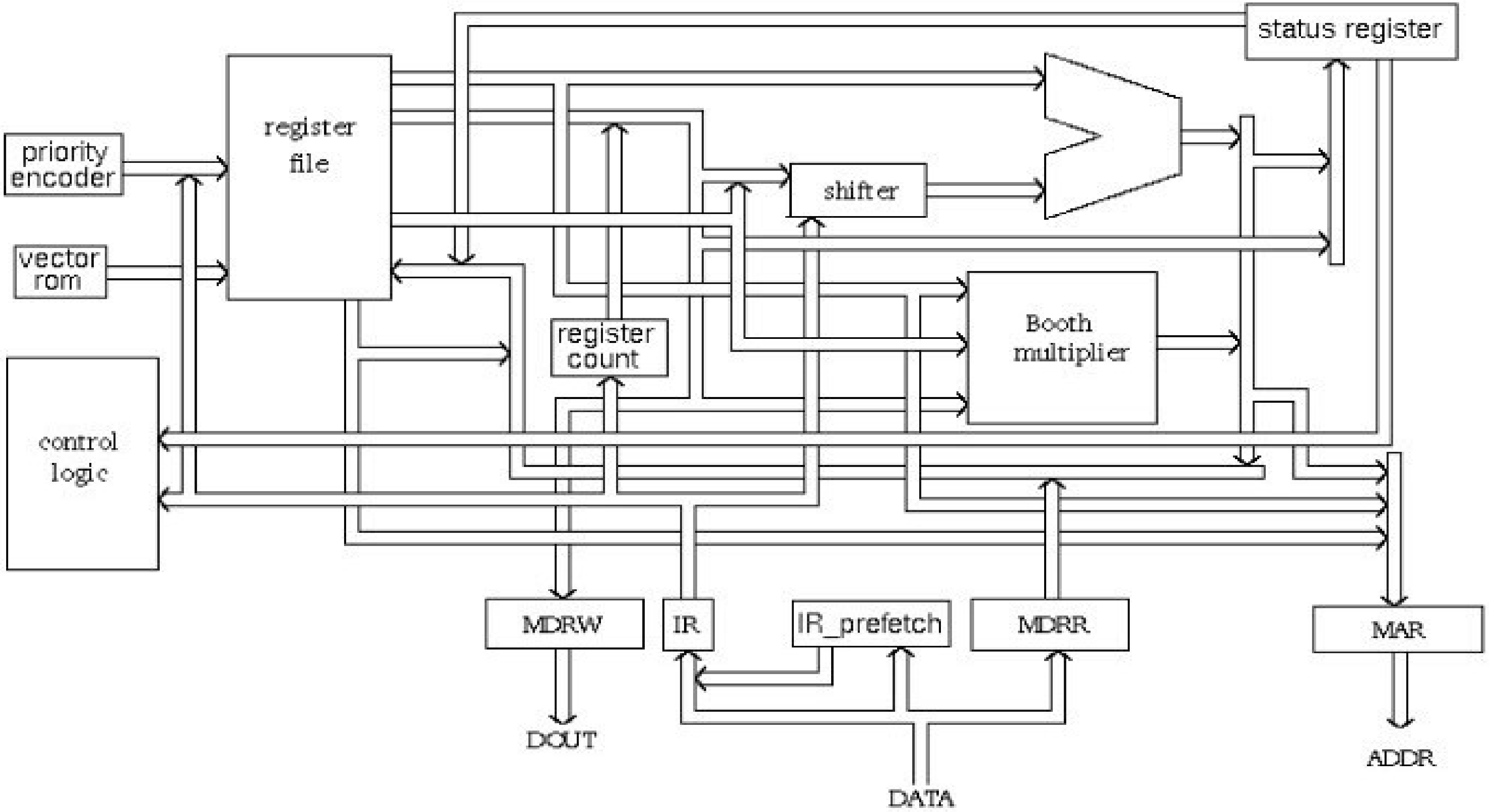
UNIT-V

INTERFACING ARM WITH EXTERNAL PERIPHERALS

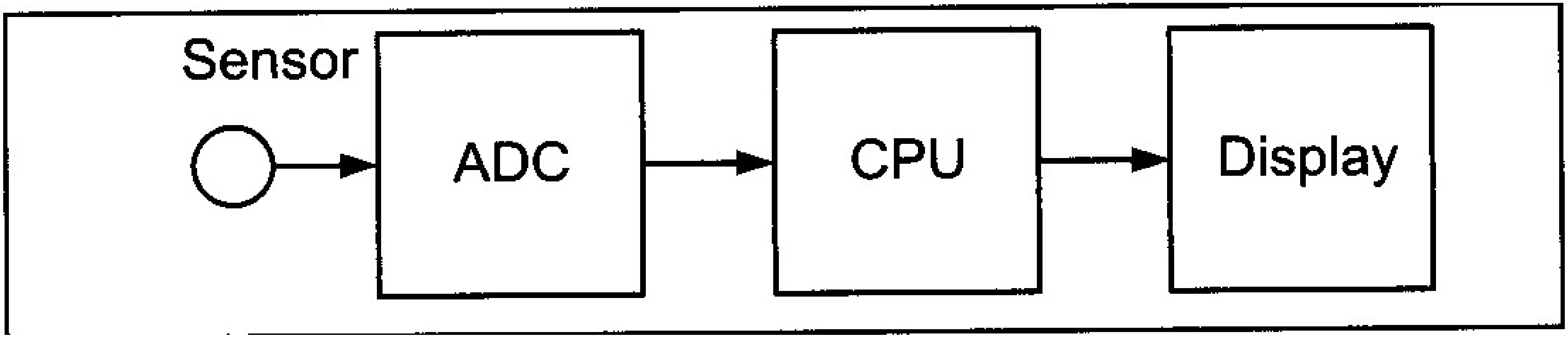
TOPICS

- Interfacing of
  - ADC
  - DAC
  - LEDs
  - Switches
  - Relays
  - LCD
  - Stepper Motor
  - Real Time Clock
  - Serial Communication
  - GSM and GPS

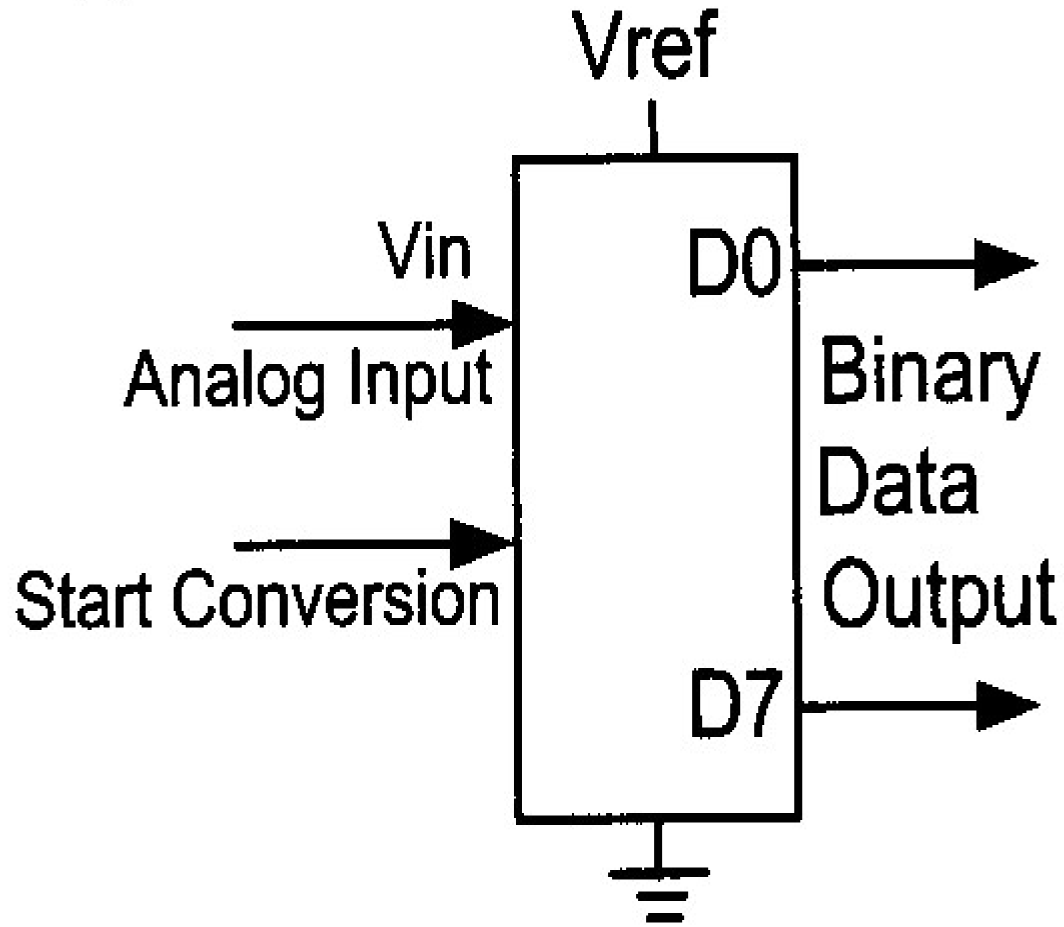
ARM Block Diagram



Sensor Connection



8-Bit ADC Block Diagram



Resolution versus Step Size

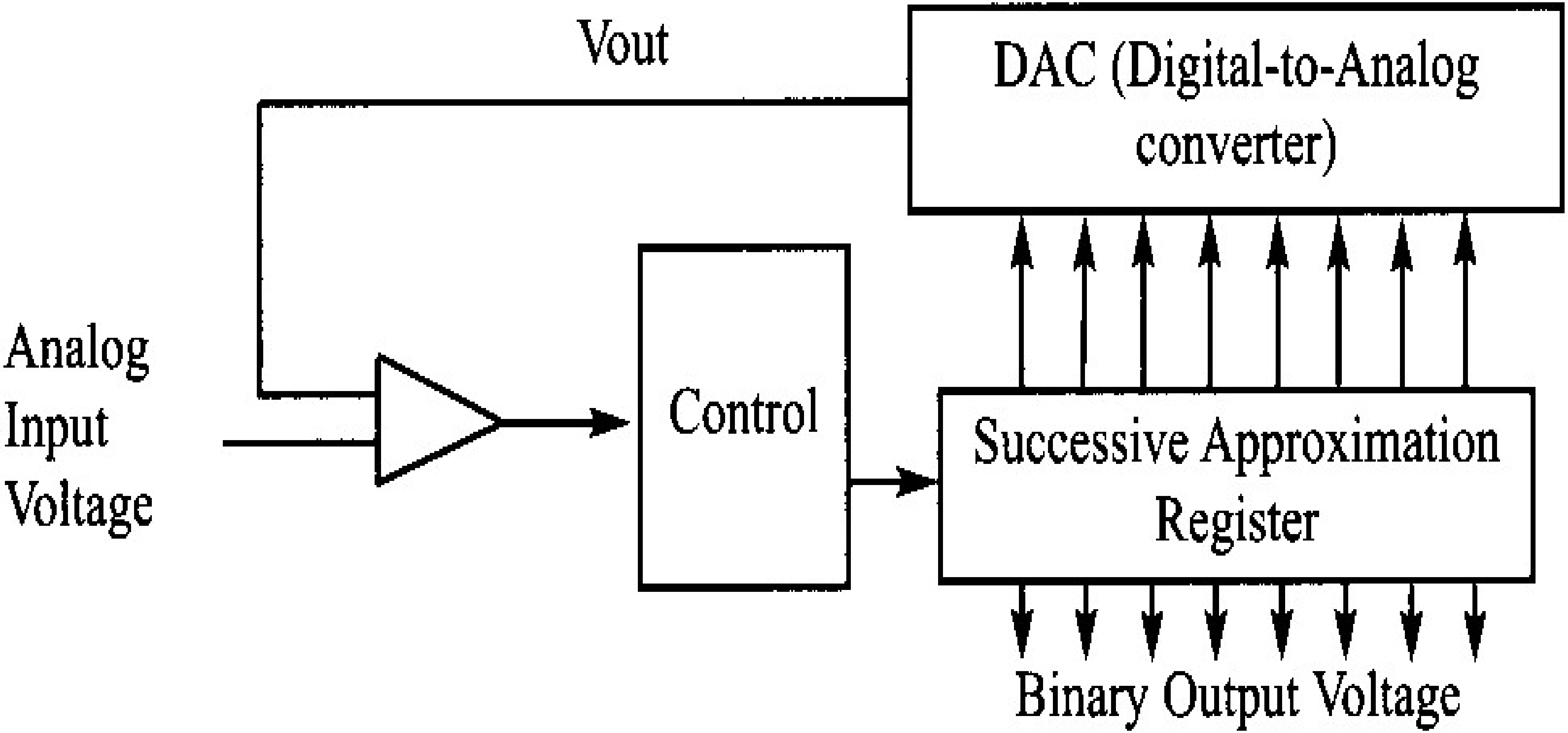
n-bit	Number of steps	Step size (mV)
8	256	5/256 = 19.53
10	1024	5/1024 = 4.88
12	4096	5/4096 = 1.2
16	65,536	5/65,536 = 0.076

Characteristics of ADC

- Resolution
- Conversion Time
- V_{ref}
- D_{out}

$$D_{out} = \frac{V_{in}}{step\ size}$$

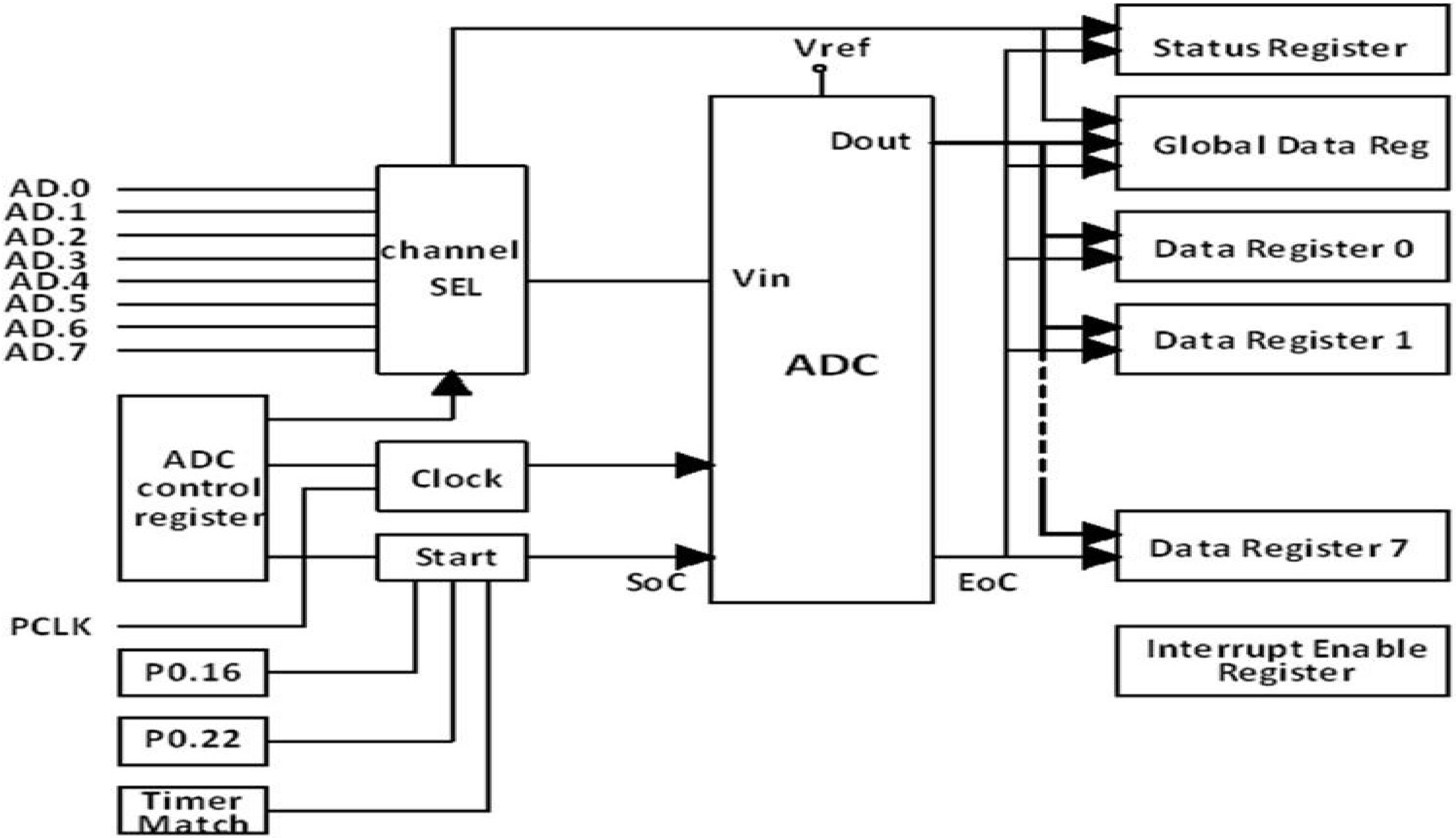
Successive Approximation ADC



Features of ADC in LPC2148

- 2 internal ADC's -ADC0 (6Channel), ADC1(8 Channel)
- Type: 10-bit, Successive Approximation type,
- Supports burst mode (repeated conversion at 3-bit to10-bit resolution)
- Supports simultaneous conversion on both ADC's
- Conversion time: 2.44 micro-seconds
- Start of Conversion by software control /on timer match/transition on a pin
- Range: 0V– VREF (+3.3 V)
- Max. clock frequency is 4.5 MHz, (by programming ADC Control (ADxCON Register)

On Chip ADC in LPC2148 Block Diagram



AD0CR (ADC0 Control Register)

31 – 28	27	26 – 24	23 – 22	21	20	19 – 17	16	15 – 8	7 –
RESERVED	EDGE	START	RESERVED	PDN	RESERVED	CLKS	BURST	CLKDIV	SEL

- **Bits 7:0 – SEL These bits select ADC0 channel as analog input. In software-controlled mode, only one of these bits should be 1.e.g. bit 7 (10000000) selects AD0.7 channel as analog input.**

- **Bits 15:8 – CLKDIV The APB(ARM Peripheral Bus)clock is divided by this value plus one, to produce the clock for ADC. This clock should be less than or equal to 4.5MHz.**

- **Bit 16 – BURST 0 = Conversions are software controlled and require 11 clocks 1 = In Burst mode ADC does repeated conversions at the rate selected by the CLKS field for the analog inputs selected by SEL field. It can be terminated by clearing this bit, but the conversion that is in progress will be completed. When Burst = 1, the START bits must be 000, otherwise the conversions will not start.**

AD0CR (ADC0 Control Register)

- **Bits 19:17 – CLKS Selects the number of clocks used for each conversion in burst mode and the number of bits of accuracy of Result bits of AD0DR. e.g. 000 uses 11 clocks for each conversion and provide 10 bits of result in corresponding ADDR register. 000 = 11 clocks / 10 bits .**
- **001 = 10 clocks / 9 bits 010 = 9 clocks / 8 bits 011 = 8 clocks / 7 bits 100 = 7 clocks / 6 bits 101 = 6 clocks / 5 bits 110 = 5 clocks / 4 bits 111 = 4 clocks / 3 bits**
- **Bit 20 – RESERVED**
- **Bit 21 – PDN 0 = ADC is in Power Down mode 1 = ADC is operational**
- **Bit 23:22 – RESERVED**
- **Bit 26:24 – START When BURST bit is 0, these bits control whether and when A/D conversion is started 000 = No start (Should be used when clearing PDN to 0) 001 = Start conversion now 010 = Start conversion when edge selected by bit 27 of this register occurs on CAP0.2/MAT0.2 pin 011= Start conversion when edge selected by bit 27 of this register occurs on CAP0.0/MAT0.0 pin 100 = Start conversion when edge selected by bit 27 of this register occurs on MAT0.1 pin 101 = Start conversion when edge selected by bit 27 of this register occurs on MAT0.3 pin 110 = Start conversion when edge selected by bit 27 of this register occurs on MAT1.0 pin 111 = Start conversion when edge selected by bit 27 of this register occurs on MAT1.1 pin**
- **□ Bit 27 – EDGE This bit is significant only when the Start field contains 010-111. In these cases, 0 = Start conversion on a rising edge on the selected CAP/MAT signal 1 = Start conversion on a falling edge on the selected CAP/MAT signal**
- **□ Bit 31:28 – RESERVED**

AD0GDR (ADC0 Global Data Register)

31	30	29 27	26 24	23 16	15 6	5
DONE	OVERRUN	RESERVED	CHN	RESERVED	RESULT	RESERVED

- **Bit 5:0 – RESERVED**
- **Bits 15:6 – RESULT When DONE bit is set to 1, this field contains 10-bit ADC result that has a value in the range of 0 (less than or equal to VSSA) to 1023 (greater than or equal to VREF).**
- **Bit 23:16 – RESERVED**
- **Bits 26:24 – CHN These bits contain the channel from which ADC value is read. e.g. 000 identifies that the RESULT field contains ADC value of channel 0.**
- **Bit 29:27 – RESERVED**
- **Bit 30 – Overrun This bit is set to 1 in burst mode if the result of one or more conversions is lost and overwritten before the conversion that produced the result in the RESULT bits. This bit is cleared by reading this register.**
- **Bit 31 – DONE This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read and when the AD0CR is written. If AD0CR is written while a conversion is still in progress, this bit is set and new conversion is started.**

ADGSR (ADC Global Start Register)

1 28	27	26 24	23 17	16	15
RESERVED	EDGE	START	RESERVED	BURST	RESERVED

- **BURST (Bit 16), START (Bit <26:24>) & EDGE (Bit 27) These bits have same function as in the individual ADC control registers i.e. AD0CR & AD1CR. Only difference is that we can use these function for both ADC commonly from this register.**

AD0STAT (ADC0 Status Register)

31 – 17	16	15 – 8	7 – 0
RESERVED	ADINT	OVERRUN7 - OVERRUN0	DONE7 - DONE0

- **Bit 7:0 – DONE7:DONE0 These bits reflect the DONE status flag from the result registers for A/D channel 7 - channel 0.**
- **Bit 15:8 – OVERRUN7:OVERRUN0 These bits reflect the OVERRUN status flag from the result registers for A/D channel 7 - channel 0.**
- **Bit 16 – ADINT This bit is 1 when any of the individual A/D channel DONE flags is asserted and enables ADC interrupt if any of interrupt is enabled in AD0INTEN register.**
- **Bit 31:17 – RESERVED**

AD0INTEN (ADC0 Interrupt Enable)

1	17	8	7	6	5	4	3	2	1	0
RESERVED		ADGINTEN	ADINT EN7	ADINT EN6	ADINT EN5	ADINT EN4	ADINT EN3	ADINT EN2	ADINT EN1	ADI EN

- **Bit 0 – ADINTEN0 0 = Completion of a A/D conversion on ADC channel 0 will not generate ar interrupt 1 = Completion of a conversion on ADC channel 0 will generate an interrupt**
- Remaining **ADINTEN bits have similar description as given for ADINTEN0.**
- **Bit 8 – ADGINTEN 0 = Only the individual ADC channels enabled by ADINTEN7:0 will generate interrupts 1 = Only the global DONE flag in A/D Data Register is enabled to generate an interrupt**

AD0DR0 – AD0DR7 (ADC0 Data Register)

31	30	29 16	15 6	5
DONE	OVERRUN	RESERVED	RESULT	RESERVED

- **Bit 5:0 – RESERVED**
- **Bits 15:6 – RESULT When DONE bit is set to 1, this field contains 10-bit ADC result that has a value in the range of 0 (less than or equal to VSSA) to 1023 (greater than or equal to VREF).**
- **Bit 29:16 – RESERVED**
- **Bit 30 – Overrun This bit is set to 1 in burst mode if the result of one or more conversions is lost and overwritten before the conversion that produced the result in the RESULT bits. This bit is cleared by reading this register.**
- **Bit 31 – DONE This bit is set to 1 when an A/D conversion completes. It is cleared when this register is read**

ADC Pin Assignment in LPC2148

Block	Symbol	Description	I/O
ADC0	AD0.1	Channel1	P0.28
	AD0.2	Channel2	P0.29
	AD0.3	Channel3	P0.30
	AD0.4	Channel4	P0.25
	AD0.6	Channel6	P0.4
	AD0.7	Channel7	P0.5
ADC1	AD1.0	Channel0	P0.6
	AD1.1	Channel1	P0.8
	AD1.2	Channel2	P0.10
	AD1.3	Channel3	P0.12
	AD1.4	Channel4	P0.13
	AD1.5	Channel5	P0.15
	AD1.6	Channel6	P0.21
	AD1.7	Channel7	P0.22

Analog Values and its Digital Equivalent

Analog Input	10-bit Digital output	Digital Output in HEX
0V	0000 0000 00 B	000H
3.3V	1111 1111 11 B	3FFH

Example

For an 10-bit ADC, we have $V_{ref} = 2.56$ V. Calculate the D0–D9 output if the analo
input is: (a) 0.2 V, and (b) 0 V. How much is the variation between (a) and (b)?

DAC in LPC2148

- LPC2148 has one10-bit DAC
- Settling time software selectable
- DAC output can drive max of 700 micro-Ampere or 350 micro-Ampere
- DAC peripheral has only one register, DACR

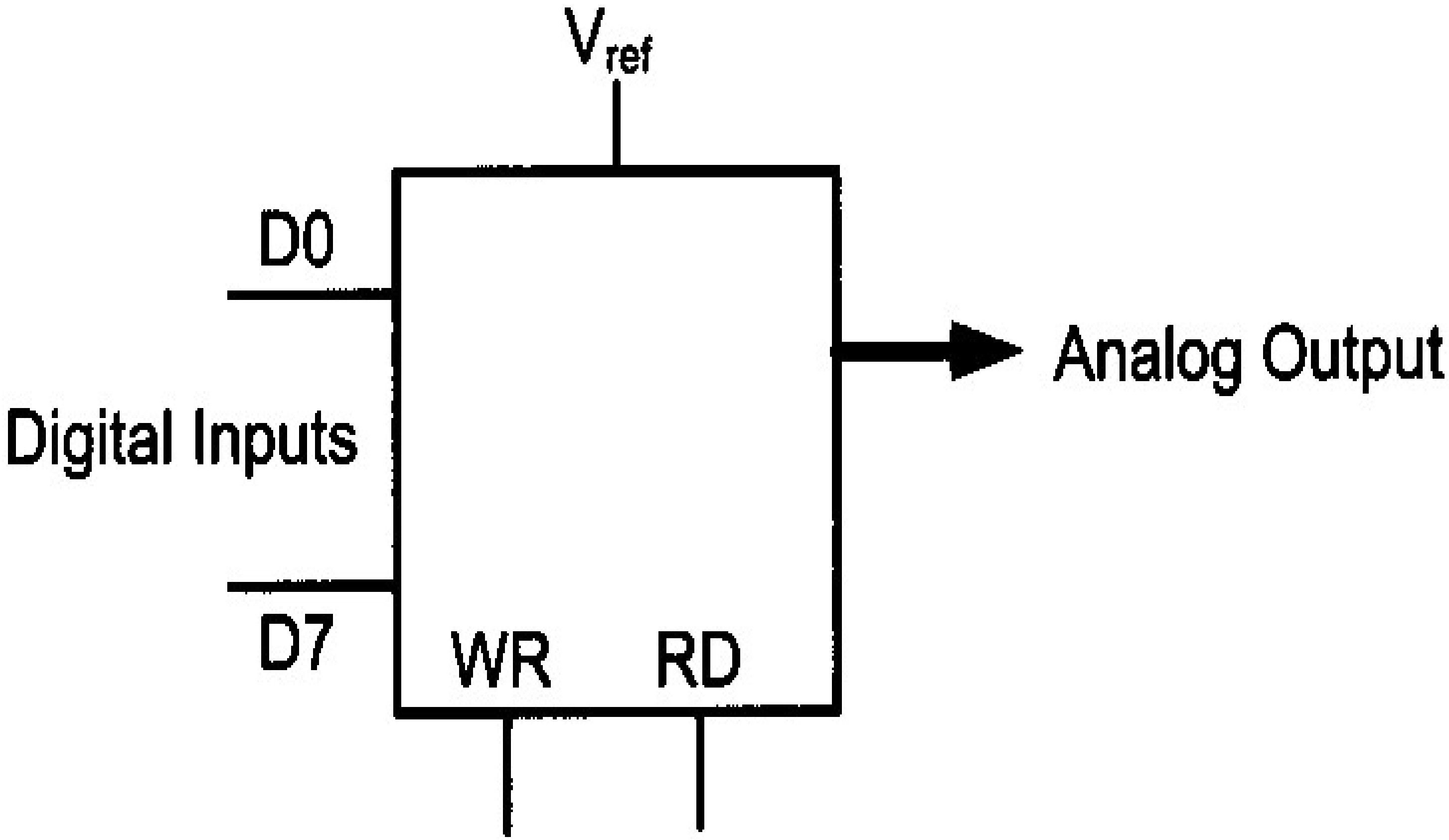
DAC Pin Description

Pin	Type	Description
AOUT	Output	Analog Output. After the selected settling time after the DACR is written with a new value, the voltage on this pin (with respect to VSSA) is VALUE/1024 * VREF.
VREF	Reference	Voltage Reference. This pin provides a voltage reference level for the D/A converter.
VDDA, VSSA	Power	Analog Power and Ground. These should be nominally the same voltages as V3 and VSSD, but should be isolated to minimize noise and error.

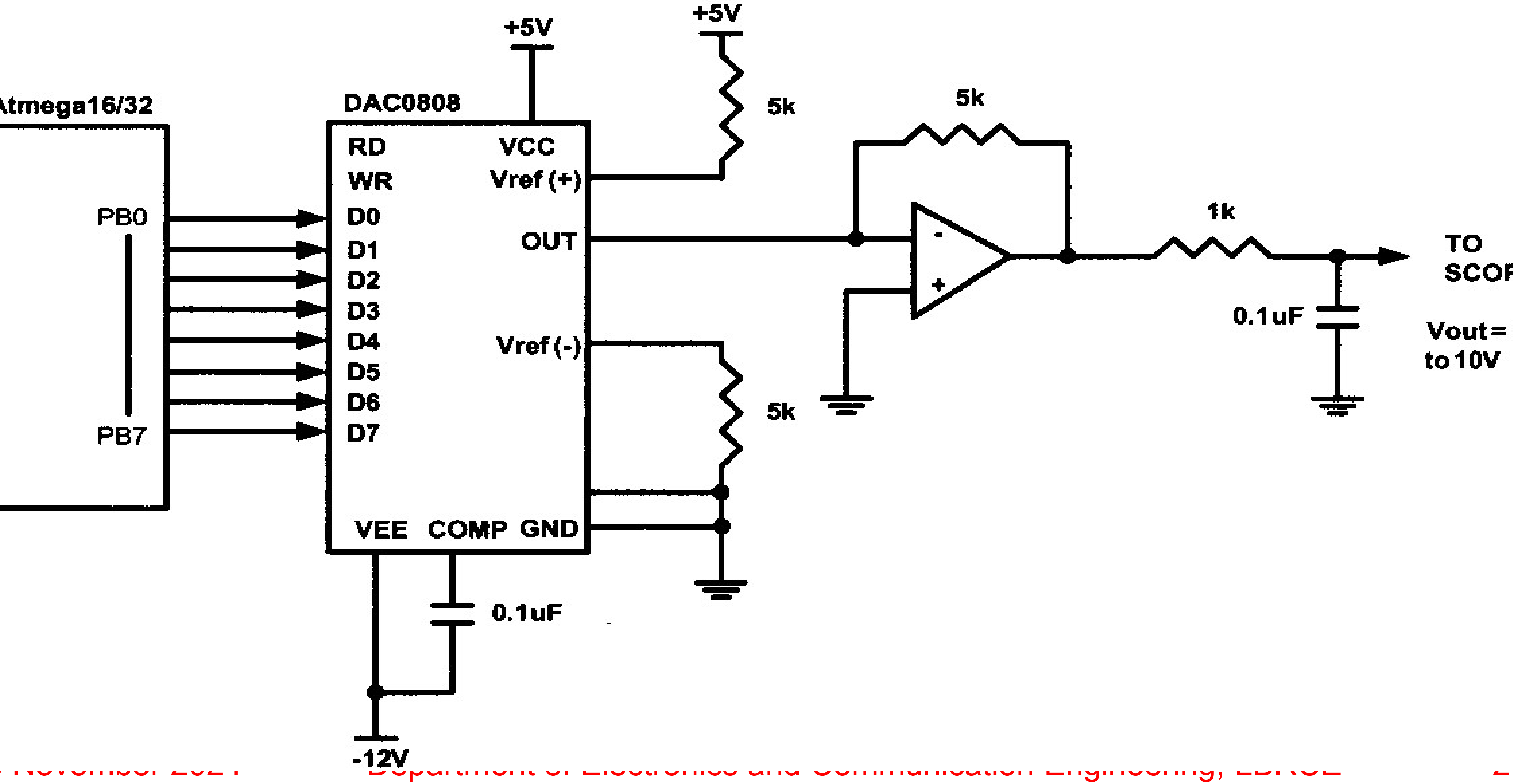
DAC Register

31 – 17	16	15 – 6	5 – 0
Reserved	BIAS	10-Bit Digital Value	Reserved

DAC Block Diagram

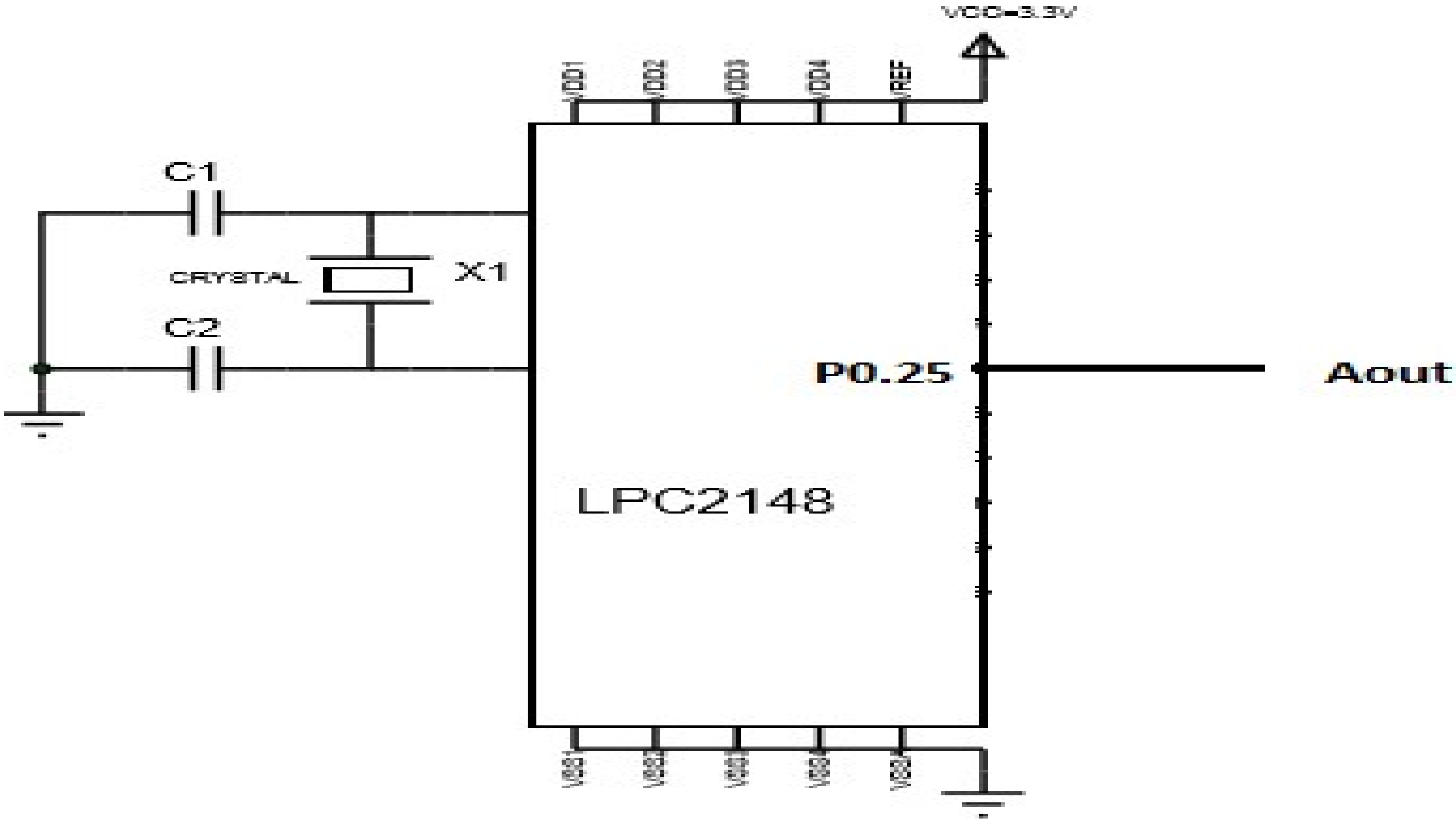


DAC 0808



Atmega16/32
PB0
PB7
DAC0808
+5V
+5V
RD
WR
D0
D1
D2
D3
D4
D5
D6
D7
VCC
Vref (+)
OUT
Vref (-)
VEE
COMP
GND
5k
5k
5k
1k
0.1uF
0.1uF
-12V
TO
SCOP
Vout=
to 10V

DAC in LPC2148



$$I_{out} = I_{ref} \left(\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256} \right)$$

Example

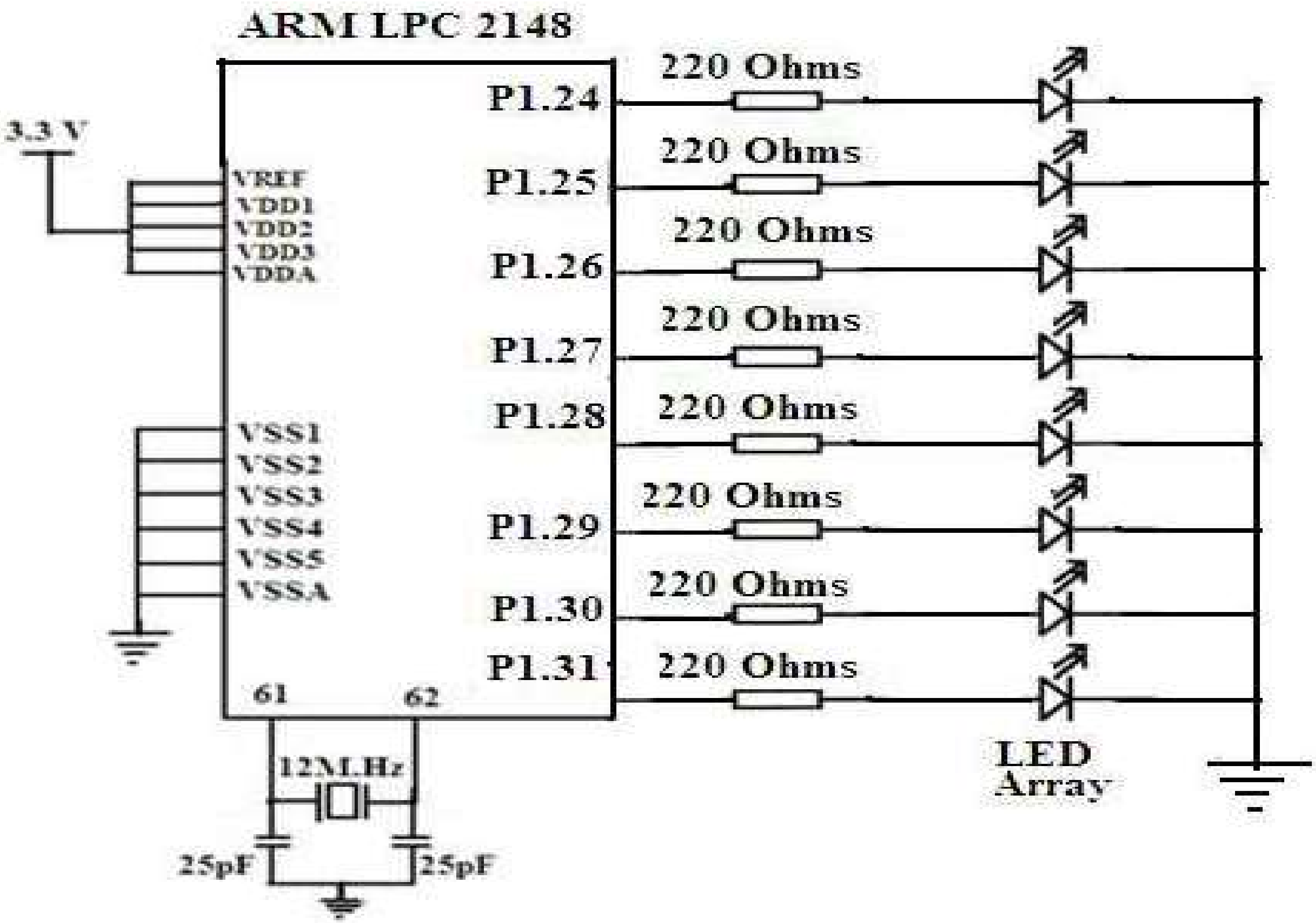
ssuming that R = 5 kilohms and I_{ref} = 2 mA, calculate V_{out} for the following binar

nputs:

) 10011001 binary (99H)

) 11001000 (C8H)

LED Interfacing



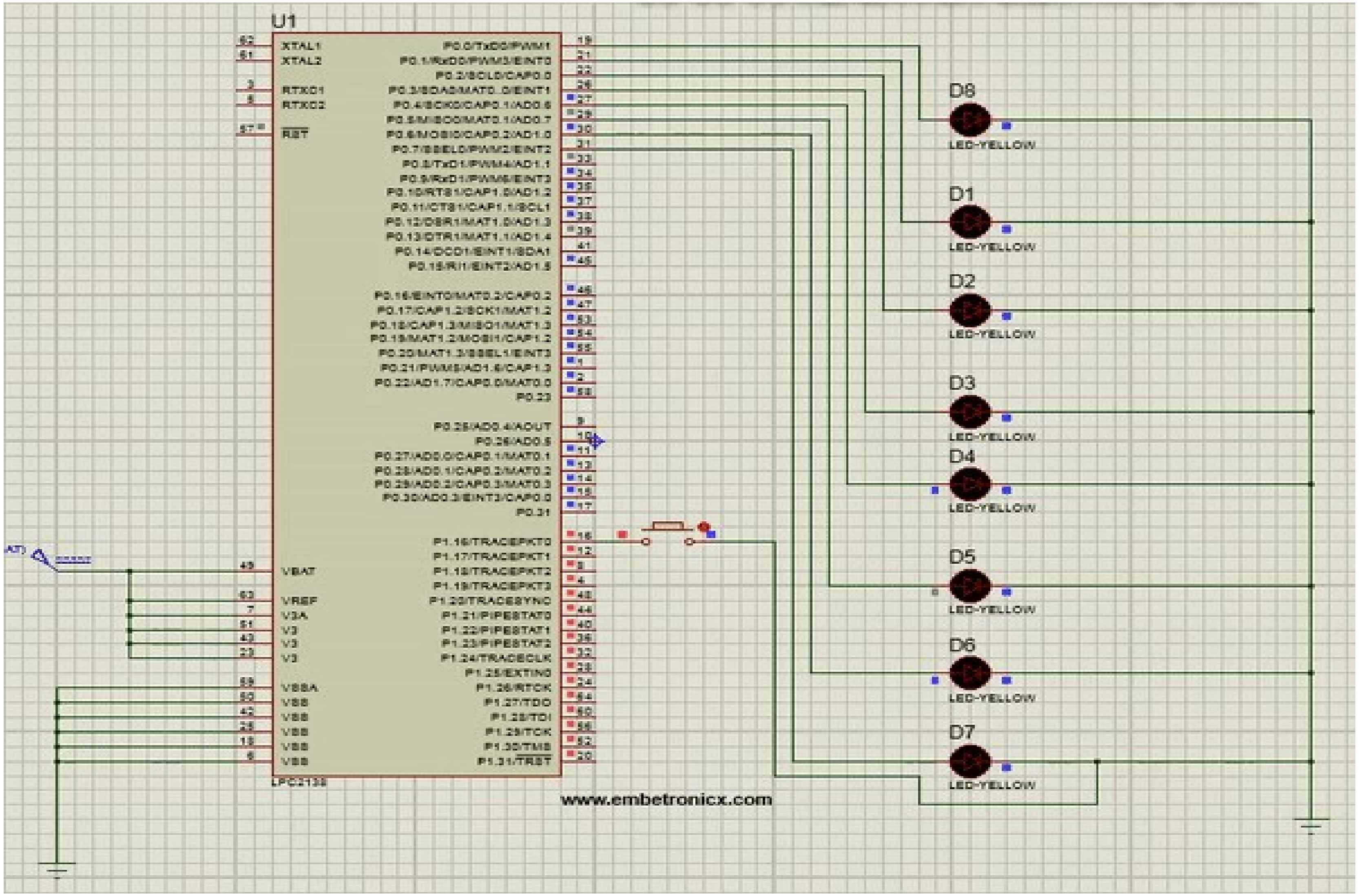
LED Interfacing Program 1

```
#include<lpc2148.H> //LPC2148 Header
void delay()
{
for(int i=0x00;i<=0xff;i++)
for(int j=0x00;j<=0xFf;j++) ; // Delay program
}
void main()
{
PINSEL2 = 0X00000000; // Set P1.24 TO P1.31 as GPIO
IO1DIR = 0XFF000000; //Port pins P1.24 to P 1.31 Configured as Output port.
while(1) //Infinite loop
{
IO1SET=0XFF000000; // Pins P1.24 to P1.31 goes to high state
delay();
IO1CLR=0XFF000000; // Pins P1.24 to P1.31 goes to low state
delay() ;
}
}
```

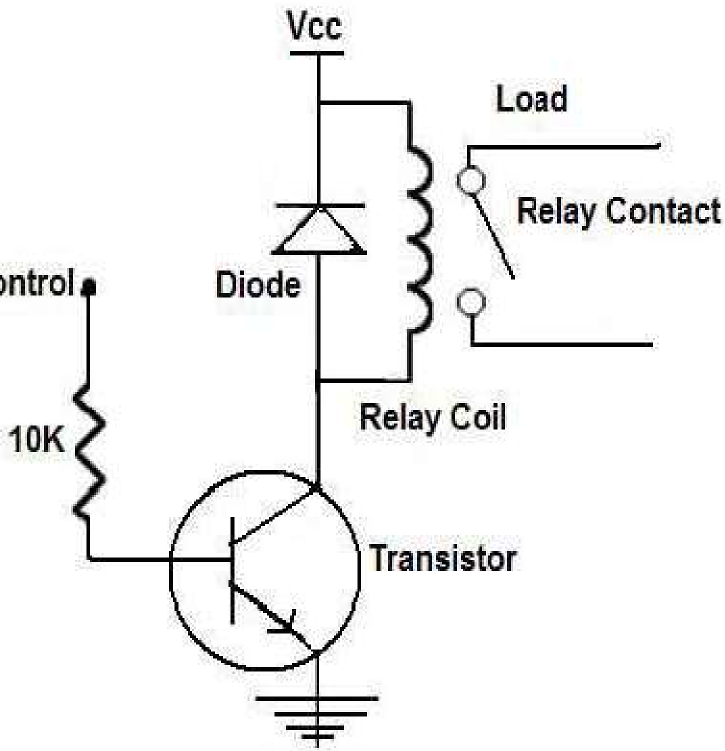
LED Interfacing Program 2

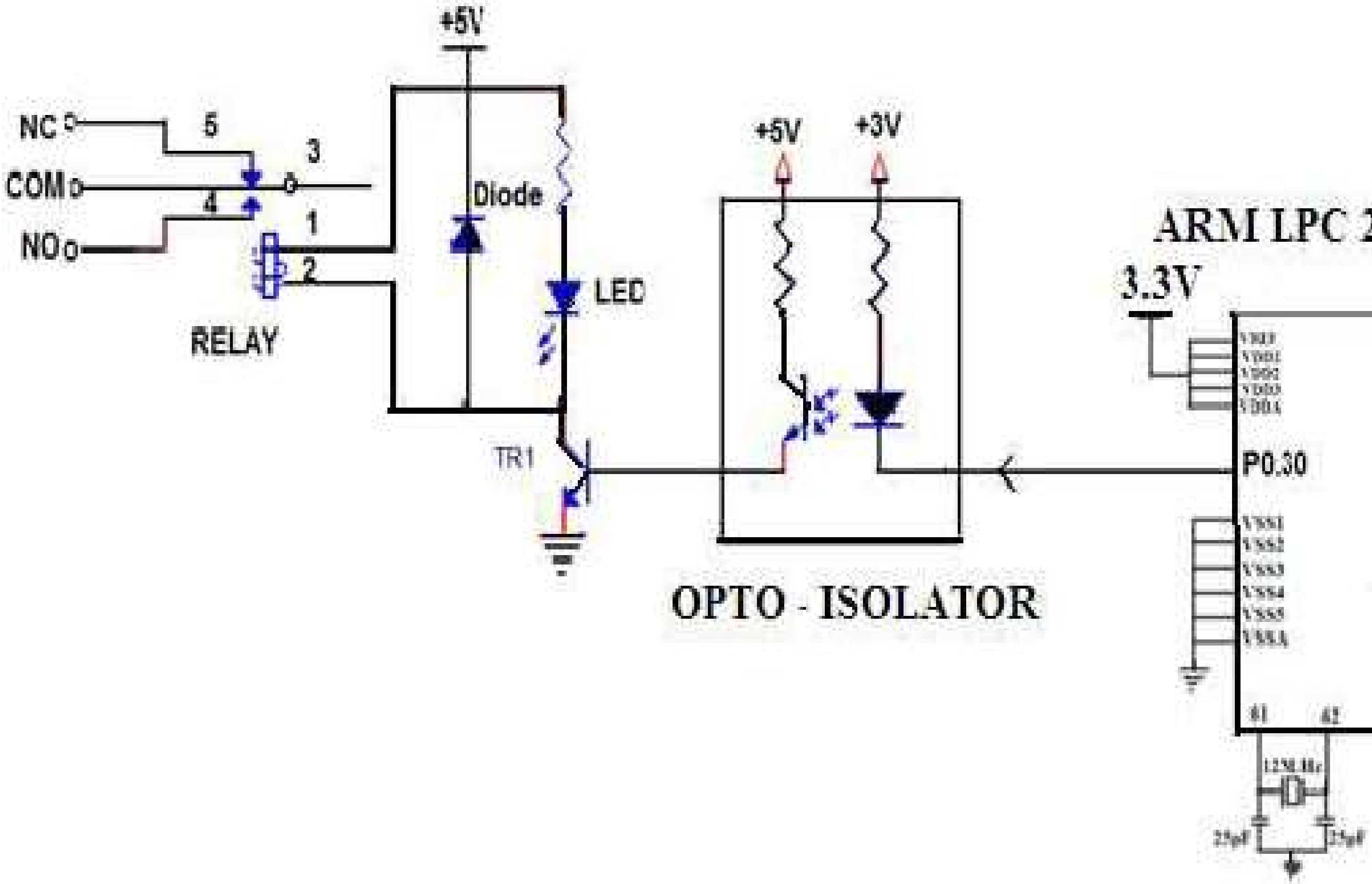
```
# include <LPC214X.H> //LPC2148 HEADER
void delay(void) // Delay Program
{
unsigned int i;
i=0xffffff;
while(i--);
}
int main(void)
{
PINSEL2=0x0000; // Port 1 is I/O
IODIR1 = 0XFF <<24 ; // Port Pins P1.24 to P1.31 as Output Pins
while(1) // Infinite loop
{
IOSET1=0X55<<25 ; // P1.25,P1.27,P1.29 & P1.31 LEDs will Glow
delay() ; // Call delay function
IOCLR1= 0X55 <<25 ; // P1.25,P1.27,P1.29 &P1.31 LEDs will be off
IOSET1=0XAA<<24 ; //P1.24,P1.26,P1.28 &P1.30 LEDs are Glow
delay () ; // Call delay function
IOCLR1=0XAA<<24 ; // P1.24,P1.26,P1.28 &P1.30 LEDs are off
}
}
```

Switch Interfacing



Relay Interfacing

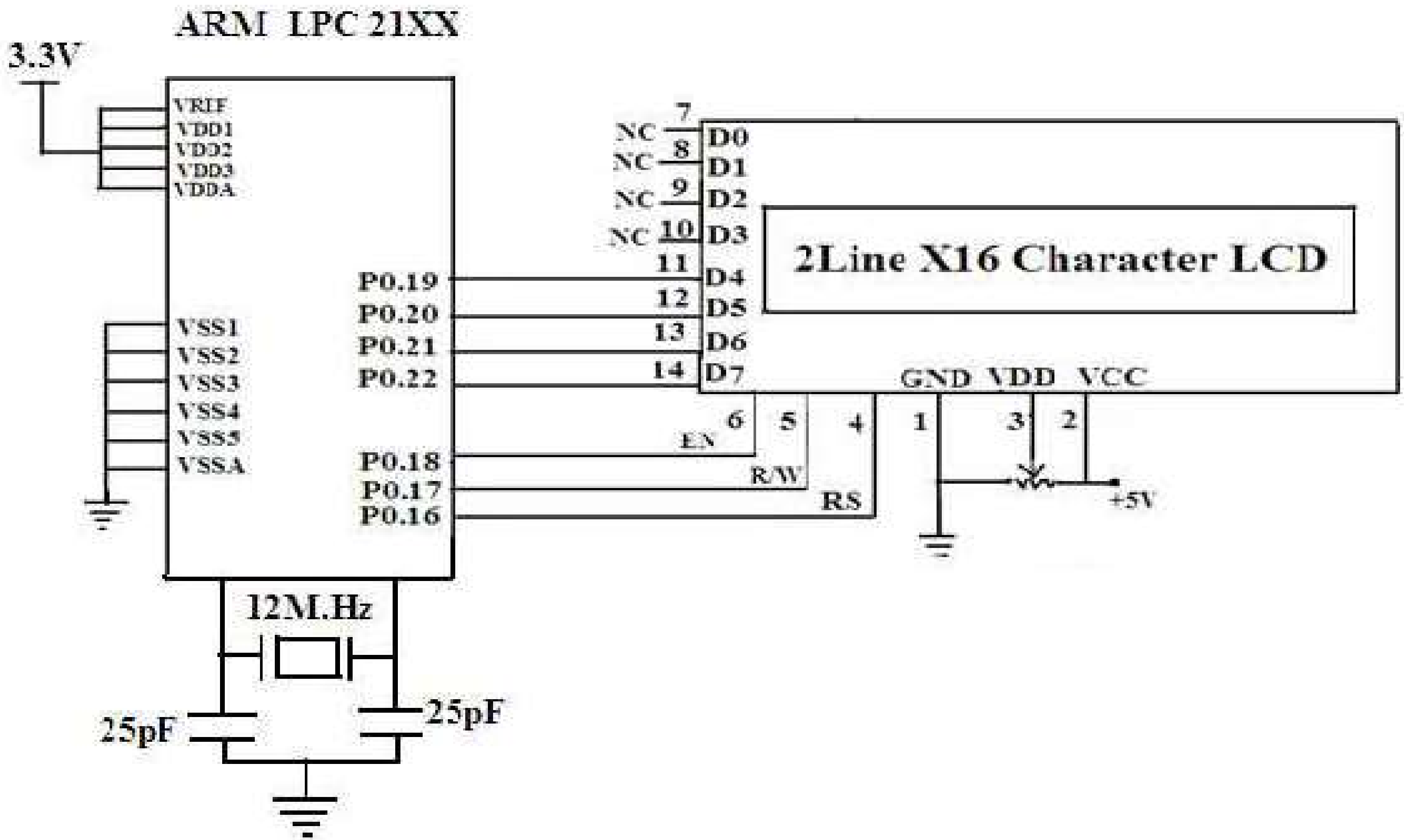




Relay Interfacing Program

```
# include <LPC214X.H> //LPC2148 HEADER
# define relay 1<<30 // ASSIGN P0.30 Pin to RELAY input PIN
void DELAY(void) // Delay function
{
unsigned int i;
i=0xffffff;
while(i--) ;
}
int main(void) // Main program
{
IODIR0=1<<30 ; // P0.30 Port Pin as Outport
while(1) //INFINITE LOOP
{
IOSET0=1<<30 ; //SWITCH OFF RELAY
DELAY() ; //CALL DELAY
IOCLR0=1<<30 ; // SWITCH ON RELAY
DELAY() ; // CALL DELAY
} // REPEAT LOOP
}
```

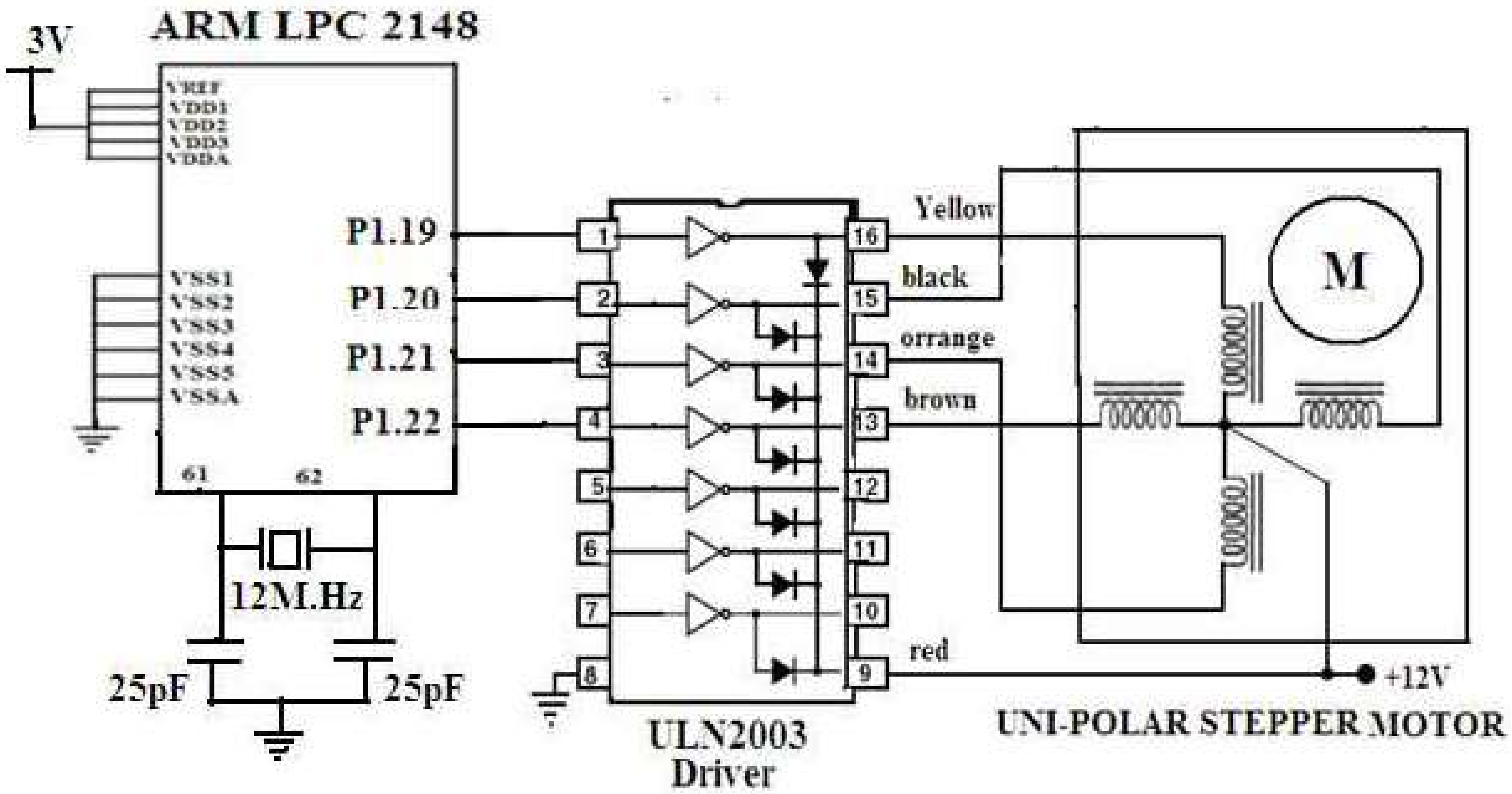
LCD Interfacing



LCD Interfacing

- 1 & 16: Ground
- 2 & 15: Vcc
- 3: Potentiometer
- 4: RS (P0.16)
- 5: R/W (P0.17)
- 6: EN (P0.18)
- 7 – 14: Data Lines (D0 – D7)
- LCD is used in 4-Bit mode
- MSB first then LSB
- P0.16 to P0.22: Data and Control signals (P0.19 – P0.22: D4 – D7)

Stepper Motor Interfacing



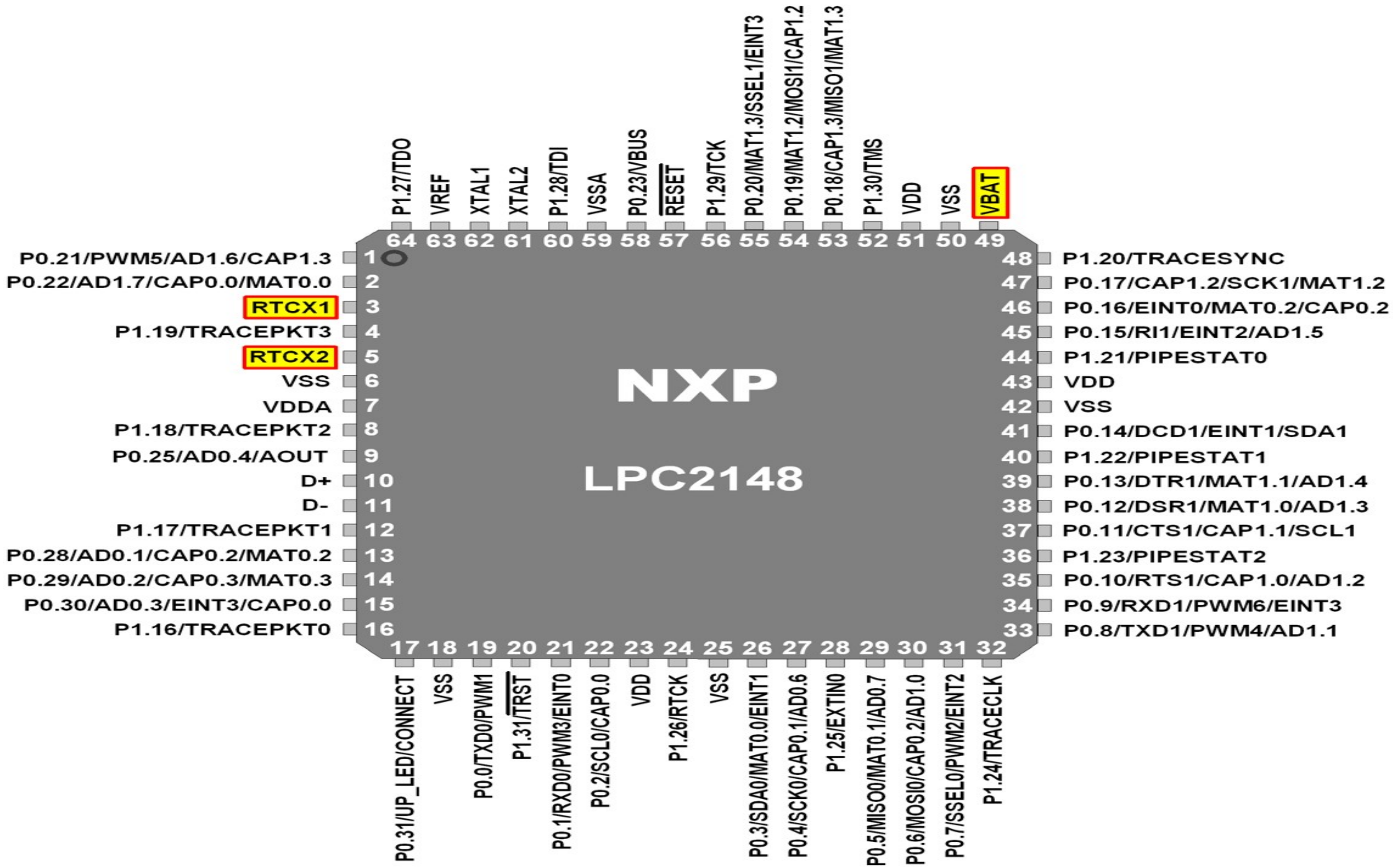
Stepper Motor Interfacing Program

```
# include <LPC214X.H> // LPC2148 HEADER
void delay_ms() ; // Delay function
void main() ; // Main program starts
{
PINSEL2 = 0X00000000; // Set P1.19 TO P1.22 as GPIO
IO1DIR=0x000000F0 ; // Set Port 1 as out port
while(1) // Infinite Loop
{
IO1PIN = 0X00000090; // Send the code1 for phase 1
delay_ms() ; // Call Delay
IO0PIN = 0X00000050 ; // Send the code 2 for phase 2
delay_ms() ; // Call Delay
IO1PIN = 0X00000060 ; // Send the code 3 for phase 3
delay_ms() ; // Call Delay
IO1PIN = 0X000000A0 ; // Send the code 3 for phase 3
delay_ms() ; // Call Delay
}
}
void delay_ms() // Delay function program
{
int i,j ;
for(i=0;i<0x0a;i++)
for (j=0;j<750;j++) ;
}
```

Real Time Clock (RTC) Interfacing

- LPC2148 has an inbuilt RTC. LPC2148RTC can be clocked by a separate 32.768 KHz oscillator or by a programmable prescale divider based on the APB clock.
- It maintains a calendar and clock and provides seconds, minutes, hours, month, year, day of week, day of month and day of year.
- We can easily program the RTC with the current date and time information in the case of loss time and date information due to power failure.

Real Time Clock (RTC) Interfacing



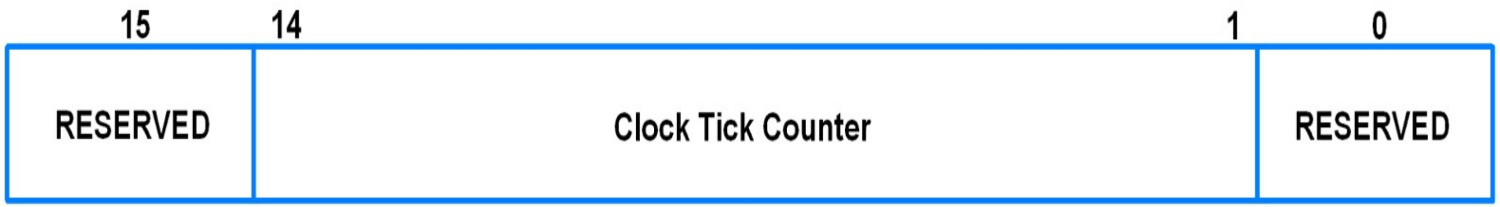
ILR (Interrupt Location Register)

7 – 2	1	0
RESERVED	RTCALF	RTCCIF

- **Bit 0 – RTCCIF**
  When this bit is 1, it means that the counter increment interrupt block generated an interrupt.
  Writing a 1 to this bit clears the counter increment interrupt. Writing a 0 has no effect.

- **Bit 1 – RTCALF**
  When this bit is 1, it means that the alarm registers generated an interrupt.
  Writing a 1 to this bit clears the alarm interrupt. Writing a 0 has no effect.

CTCR (Clock Tick Counter Register)



- It can be reset through the Clock Control Register (CCR).
- It consists of the bits of the clock divide counter.
- **Bits 14:1 – Clock Tick Counter**
  Prior to the seconds counter, the CTC counts 32,768 clocks per second. Due to RTC Prescalar, these 32,768 time increments may not all be of the same duration.

CCR (Clock Control Register)

7–5	4	3–2	1	0
RESERVED	CLKSRC	CTTEST	CTCRST	CLKEN

- **Bit 0 – CLKEEN (Clock Enable)**
  0 = Timer counters are disabled. They should be initialized in this condition.
  1 = Timer counters are enabled

- **Bit 1 – CTRST (CTC Reset)**
  When 1, elements in CTC (Clock Tick Counter) are reset. The elements remain reset until this bit is changed to 0.

- **Bit 3:2 – CTTEST (Test Enable)**
  These bits should always be 0 during normal operation.

- **Bit 4 – CLKSRC**
  0 = CTC takes clock from Prescalar
  1 = CTC takes clock from 32.768 kHz oscillator

CIIR (Counter Increment Interrupt Register)

7	6	5	4	3	2	1	0
IMYEAR	IMMON	IMDOY	IMDOW	IMDOM	IMHOUR	IMMIN	IMSEC

- **Bit 0 – IMSEC:** When 1, an increment of the Seconds value generates an interrupt.
- **Bit 1 – IMMIN:** When 1, an increment of the Minutes value generates an interrupt.
- **Bit 2 – IMHOUR:** When 1, an increment of the Hours value generates an interrupt.
- **Bit 3 – IMDOM:** When 1, an increment of the Day of Month value generates an interrupt.
- **Bit 4 – IMDOW:** When 1, an increment of the Day of Week value generates an interrupt.
- **Bit 5 – IMDOY:** When 1, an increment of the Day of Year value generates an interrupt.
- **Bit 6 – IMMON:** When 1, an increment of the Month value generates an interrupt.
- **Bit 7 – IMYEAR**: When 1, an increment of the Year value generates an interrupt.

AMR (Alarm Mask Register)

7	6	5	4	3	2	1	0
AMRYEAR	AMRMON	AMRDOY	AMRDOW	AMRDOM	AMRHOUR	AMRMIN	AMRSEC

- **Bit 0 – AMRSEC:** When 1, the Seconds value is not compared for alarm.
- **Bit 1 – AMRMIN:** When 1, the Minutes value is not compared for alarm.
- **Bit 2 – AMRHOUR:** When 1, the Hours value is not compared for alarm.
- **Bit 3 – AMRDOM:** When 1, the Day of Month value is not compared for alarm.
- **Bit 4 – AMRDOW:** When 1, the Day of Week value is not compared for alarm.
- **Bit 5 – AMRDOY:** When 1, the Day of Year value is not compared for alarm.
- **Bit 6 – AMRMON:** When 1, the Month value is not compared for alarm.
- **Bit 7 – AMRYEAR:** When 1, the Year value is not compared for alarm.

CTIME0 (Consolidated Time Register 0)

31 – 27	26 – 24	23 – 21	20 – 16	15 – 14	13 – 8	7 – 6	5 – 0
RESERVED	Day Of Weak	RESERVED	Hour	RESERVED	Minutes	RESERVED	Seconds

- **Bits 5:0 – Seconds**
  Seconds value in the range of 0 to 59.
- **Bits 13:8 – Minutes**
  Minutes value in the range of 0 to 59.
- **Bits 20:16 – Hours**
  Hours value in the range of 0 to 23.
- **Bits 26:24 – Day of Week**
  Day of Week value in the range of 0 to 6.

CTIME1 (Consolidated Time Register 1)

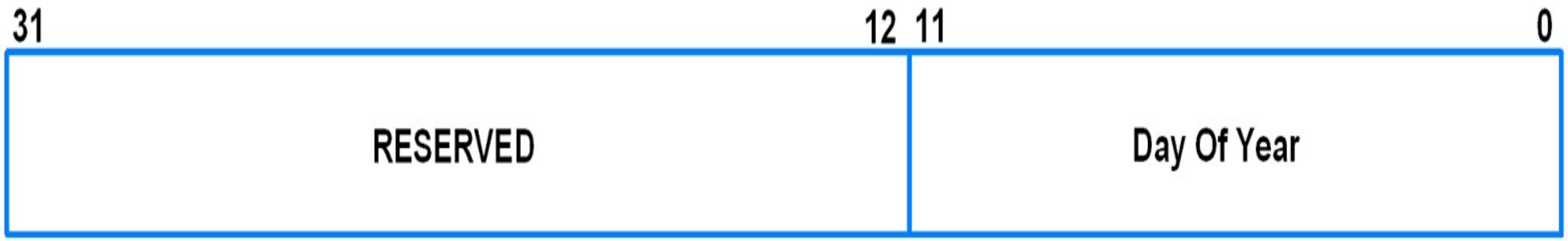
31 – 28	27 – 16	15 – 12	11 – 8	7 – 5	4 – 0
RESERVED	Year	RESERVED	Month	RESERVED	Day Of Month

- **Bits 4:0 – Day of Month**
  Day of Month value in the range of 1 to 28, 29, 30 or 31 (depending on the month and whether it is a leap year).

- **Bits 11:8 – Month**
  Month value in the range of 1 to 12.

- **Bits 27:16 – Year**
  Year value in the range of 0 to 4095

CTIME2 (Consolidated Time Register 2)



- **Bits 11:0 – Day of Year**
  Day of Year value in the range of 1 to 365 (366 for leap years).

Time Counter Group

Name	Size	Description
SEC	6	Seconds value in the range of 0 to 59
MIN	6	Minutes value in the range of 0 to 59
HOUR	5	Hours value in the range of 0 to 23
DOM	5	Day of Month value in the range of 1 to 28, 29, 30 or 31 (depending on month and whether it is a leap year)
DOW	3	Day of Week value in the range of 0 to 6
DOY	9	Day of Year value in the range of 1 to 365 (366 for leap years 0
MONTH	4	Month value in the range of 1 to 12
YEAR	12	Year value in the range of 0 to 4095

Alarm Register Group

Name	Size	Description
ALSEC	6	Alarm value for Seconds
ALMIN	6	Alarm value for Minutes
ALHOUR	5	Alarm value for Hours
ALDOM	5	Alarm value for Day of Month
ALDOW	3	Alarm value for Day of Week
ALDOY	9	Alarm value for Day of Year
ALMON	4	Alarm value for Month
ALYEAR	12	Alarm value for Year

PREINT (Prescaler Integer Register)

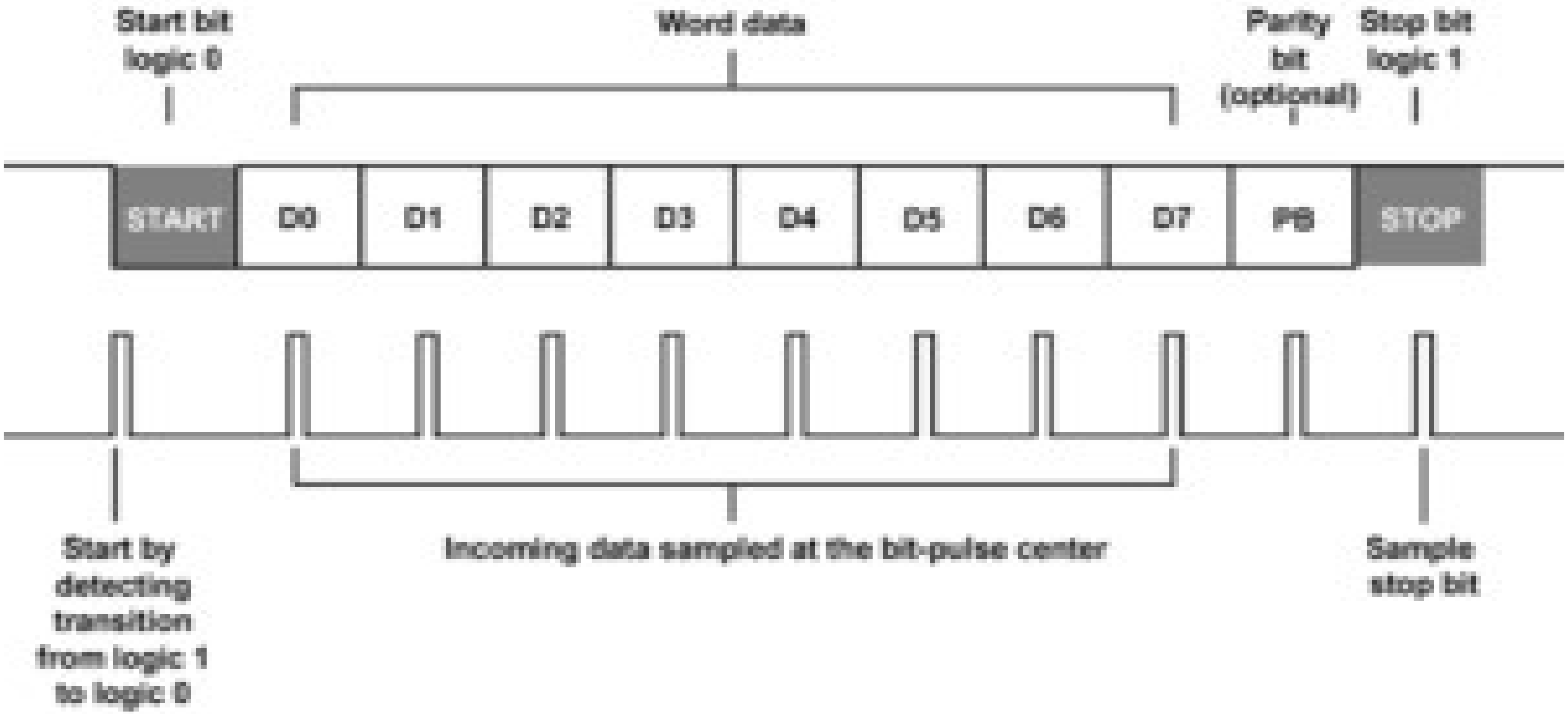
- **Bits 12:0 – Prescale Integer**
  Contains the integer value of the RTC prescaler
- **PREINT** = int (PCLK/32768) – 1
- PREINT must be greater than or equal to 1

PREFRAC (Prescaler Fraction Register)

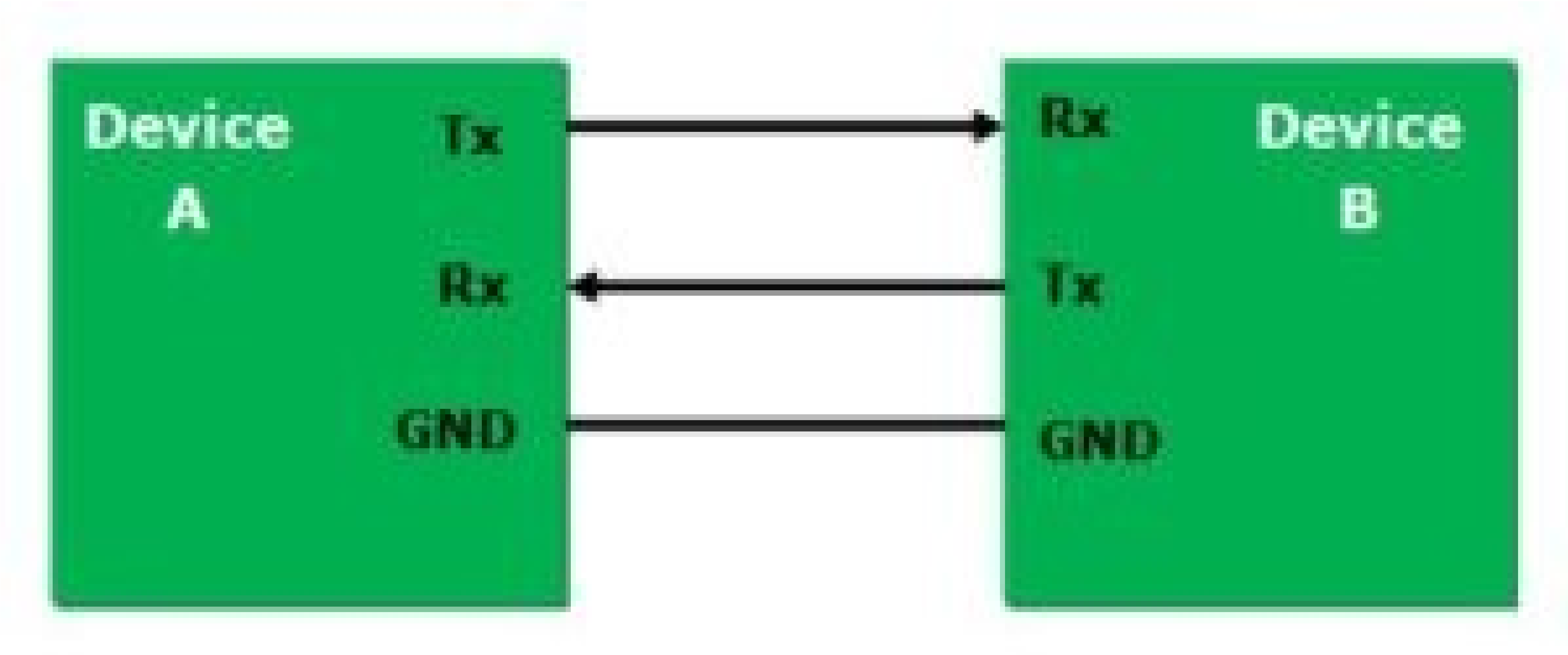
- **Bits 14:0 - Prescale Fraction**
  Contains the fraction value of the RTC prescaler.

- **PREFRAC** = PCLK – ((PREINT+1) * 32768)

Serial Communication Interfacing



Full Duplex Communication



List of UARTs in LPC2148

PINs	TxD	RxD
UART0	P0.0	P0.1
UART1	P0.8	P0.9

RS-232 Level Converter

- Most of microchips work on TTL or CMOS voltage levels which can’t be used to communicate over RS-232 protocol.
- Voltage or level converter is needed which can convert TTL to RS-232 and RS-232 to TTL voltage levels.
- The most commonly used RS-232 level converter is MAX3232 chip.

List of Registers

- **U0THR: Transmit Hold Register:** This register contains 8-bit write data which can be transmitted through UART0. This is write only register.

- **U0RBR: Receive Buffer Register:** This register contains 8-bit received data from UART0. This data is nothing but top most byte of Rx FIFO. When we use 5, 6 or 7-bit data then remaining bits are padded with 0's by default. This is read only register.

- **U0LCR: Line Control Register:** The value or settings in this register configure the UART0 block. As this is an 8-bit register. There are several parameters configured through this register such as word length, stop bit, parity enable, parity select, break control, divisor latch access bit. This register setting plays important role while initializing UART0 before using it.

- **U0DLL & U0DLM: U0DLL & U0DLM are standard** UART0 baud rate generator divider registers. Each of this register holds 8-bit values. Together these registers form a 16-bit divisor value which will be used for baud rate generation. This will be discussed further while code explanation with respect to real world example.

- **U0FDR: Fractional Divider Register:** This is another very important register, which plays significant role in baud rate generation. In this 8-bit register, first four bits i.e. **Bit[3 to 0]-DIVADDVAL:** This is the Prescale Divisor value. If this value is 0 then fractional baud rate generator have no effect on UART0 baud rate. The remaining 4-bits i.e. **Bit[4 to 7]-MULVAL:** This defines Prescale Multiplier value. Even if fractional baud rate generator is not used the value in this register must be more than or equal to '1'.

Baudrate Calculation in LPC2148

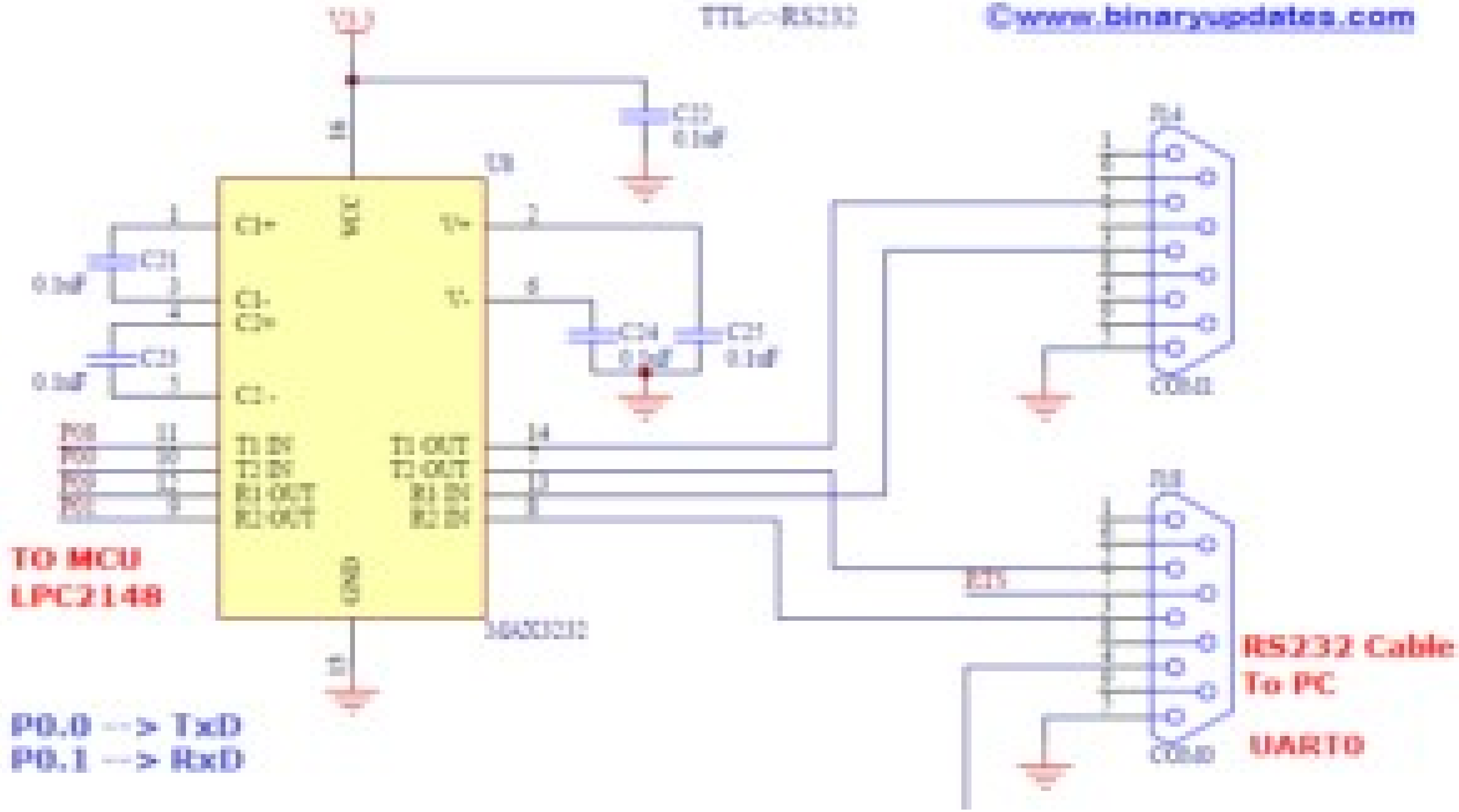
$$\text{BaudRate} = \frac{PCLK}{16 \times (256 \times U0DLM + U0DLL) \times \left(1 + \frac{DIVADDVAL}{MULVAL}\right)}$$

PCLK: Peripheral Clock Frequency (In MHz)

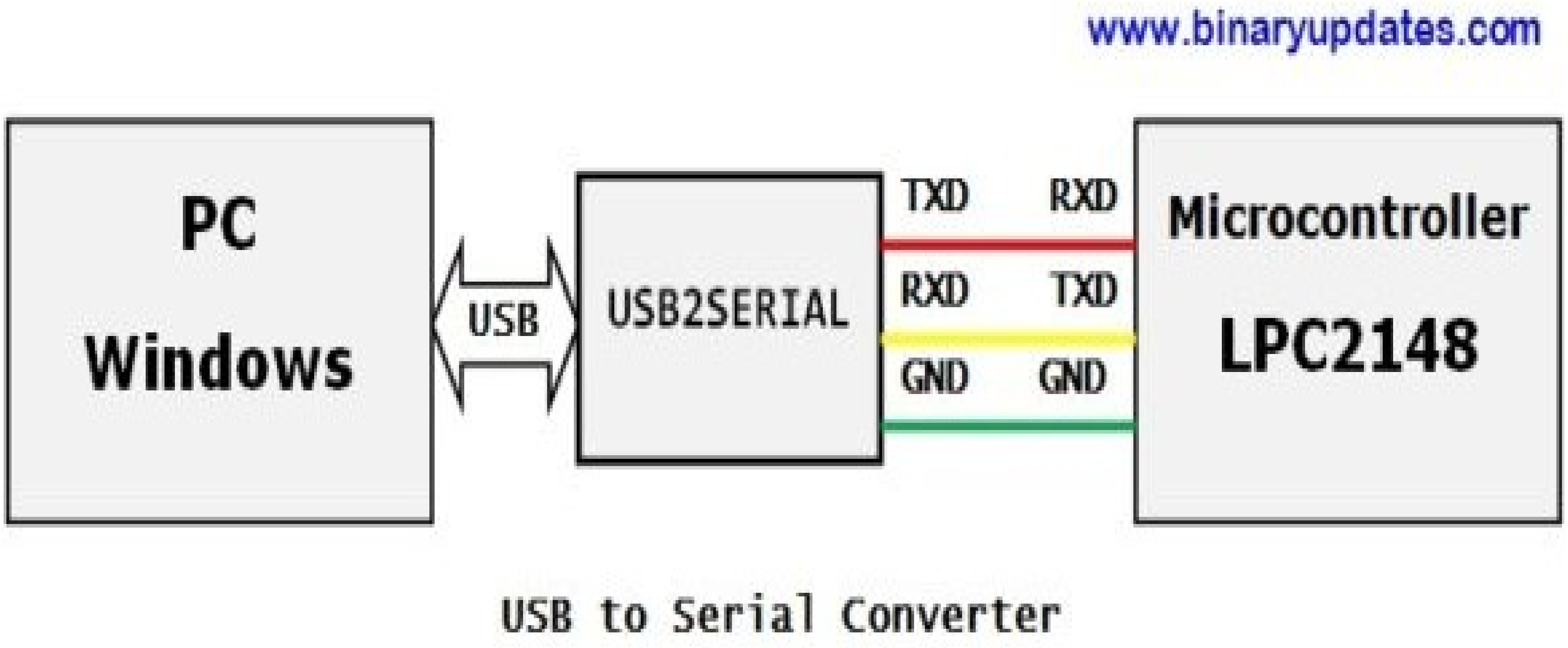
U0DLM, U0DLL: These are standard UART0 baud rate generator divider registers

MULVAL, DIVADDVAL: These registers are fraction generator values. They must meet following condition 0<MULVAL, DIVADDVAL <=15 with MULVAL=0 treated as MULVAL=1

Circuit Diagram of UART in LPC2148



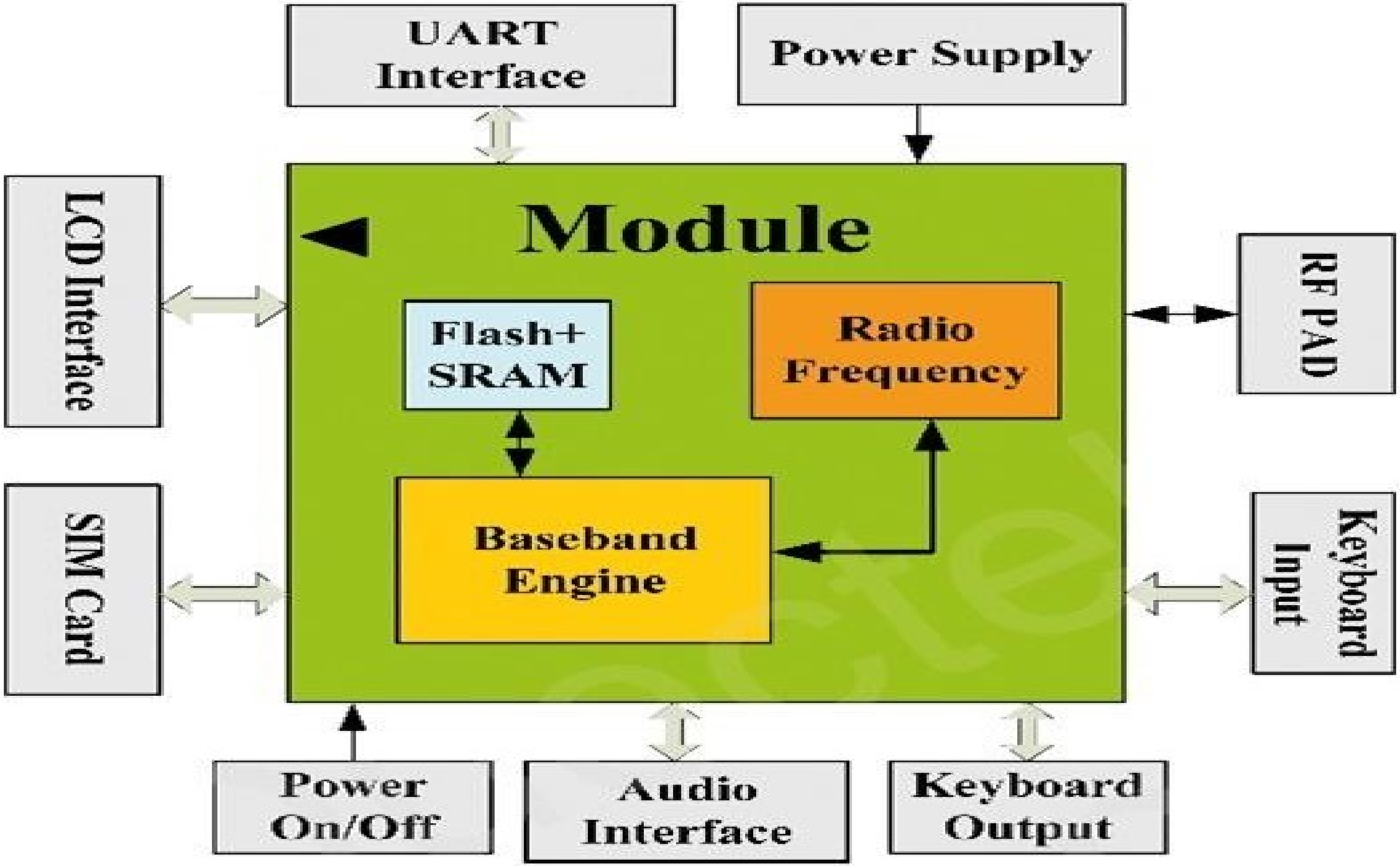
Connection between LPC2148 and PC



GSM Interfacing with LPC 2148

- GSM (Global System for Mobile Communications) is the technology that underpins most of the world's mobile phone networks.
- GSM is an open, digital cellular technology used for transmitting mobile voice and data services.
- GSM operates in the 900 MHz and 1.8 GHz bands GSM supports data transfer speeds of up to 9.6 kbps, all owing the transmission of basic data services such as SMS.

GSM Module

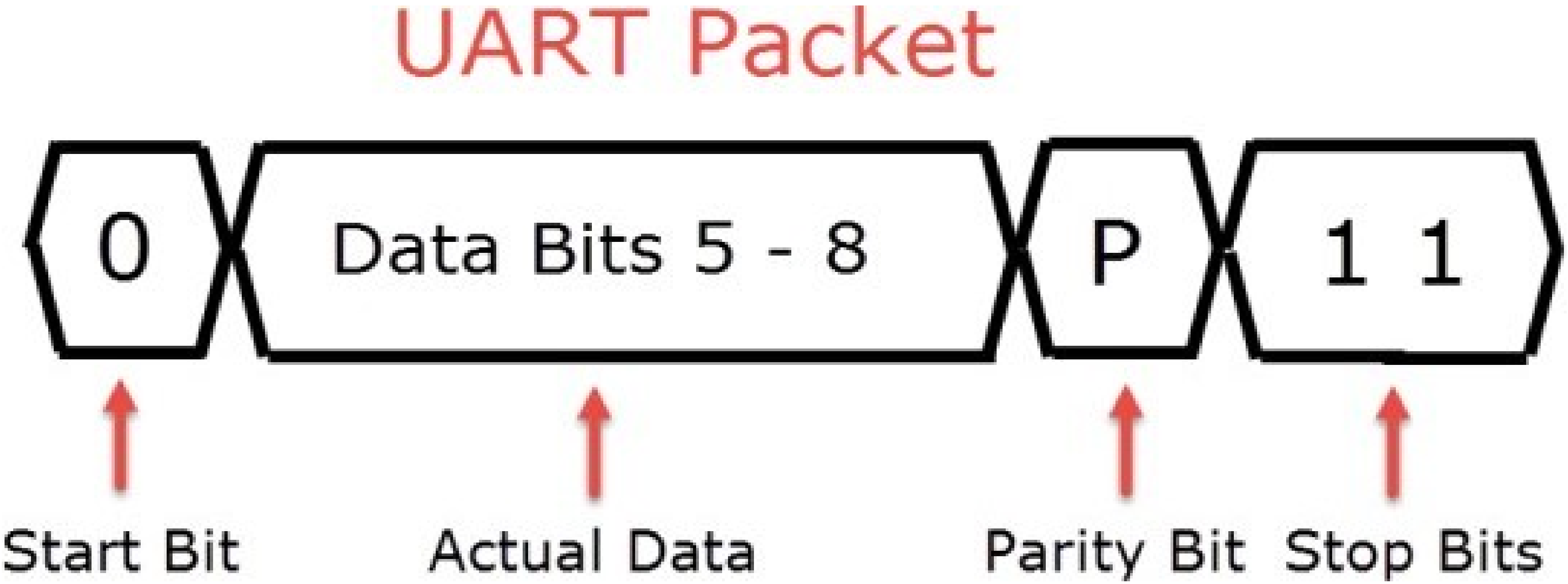


UART Interface
Power Supply
LCD Interface
Module
Flash+ SRAM
Radio Frequency
RF PAD
SIM Card
Baseband Engine
Keyboard Input
Power On/Off
Audio Interface
Keyboard Output

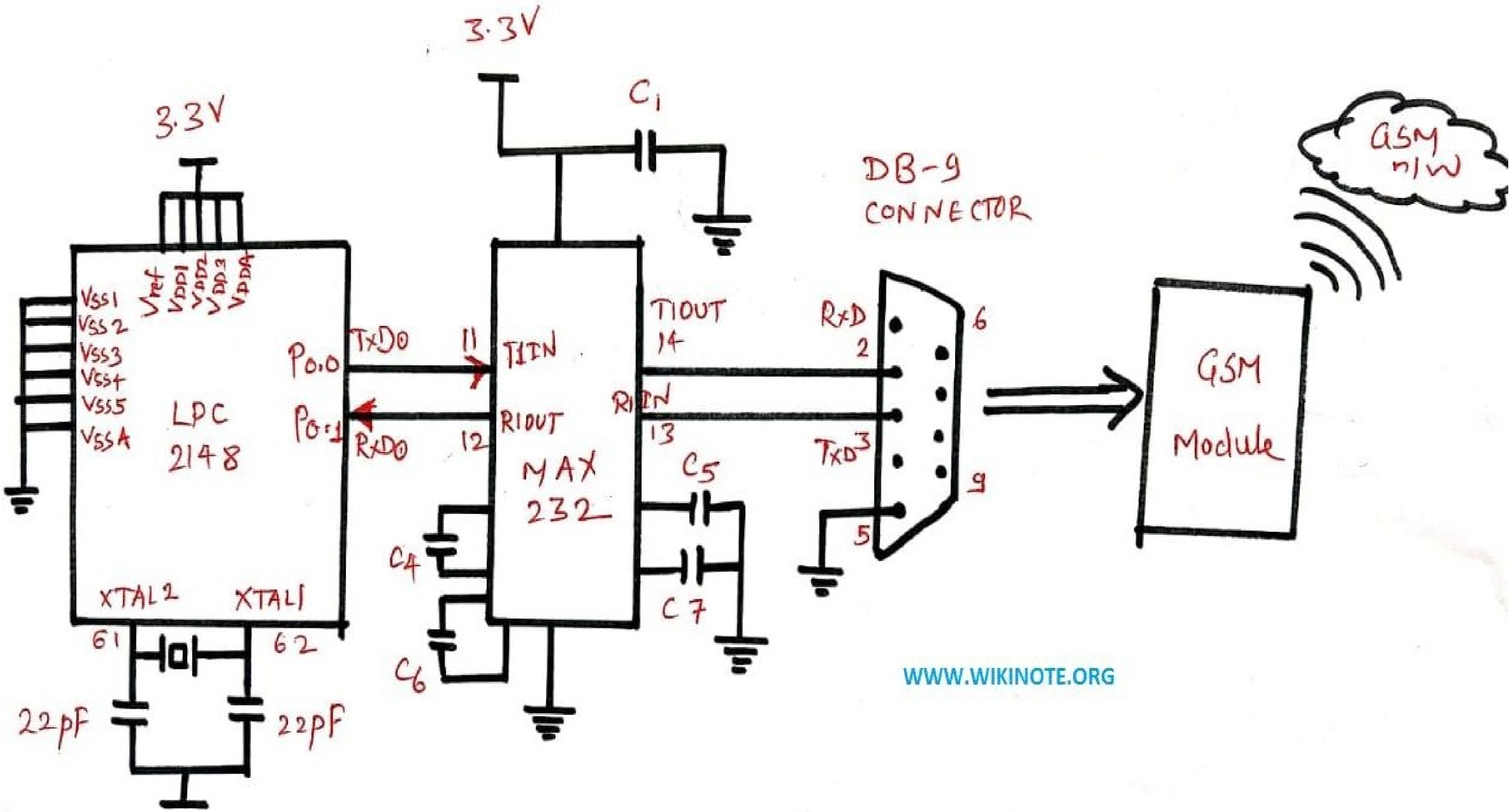
GSM AT Commands

GSMATCommandsandtheirfunctions	
ATCommand	**Functionof ATCommand**
ATD	Dial
AT+CGMS	SendSMSMessage
AT+CMSS	SendSMSMessagefrom storage
AT+CMGL	ListSMSMessages
AT+CMGR	ReadSMSMessages
AT+CSCA?	ServiceCentreAddress
AT+CPMS	TochoosestoragefromMEorSM
AT+IPR=0	Tochooseauto frombaudrate
AT+CMGF=	TochoosePDUModeorText Mode

UART Data Format



GSM Interfacing with LPC 2148



Pin Assignment with LPC 2148

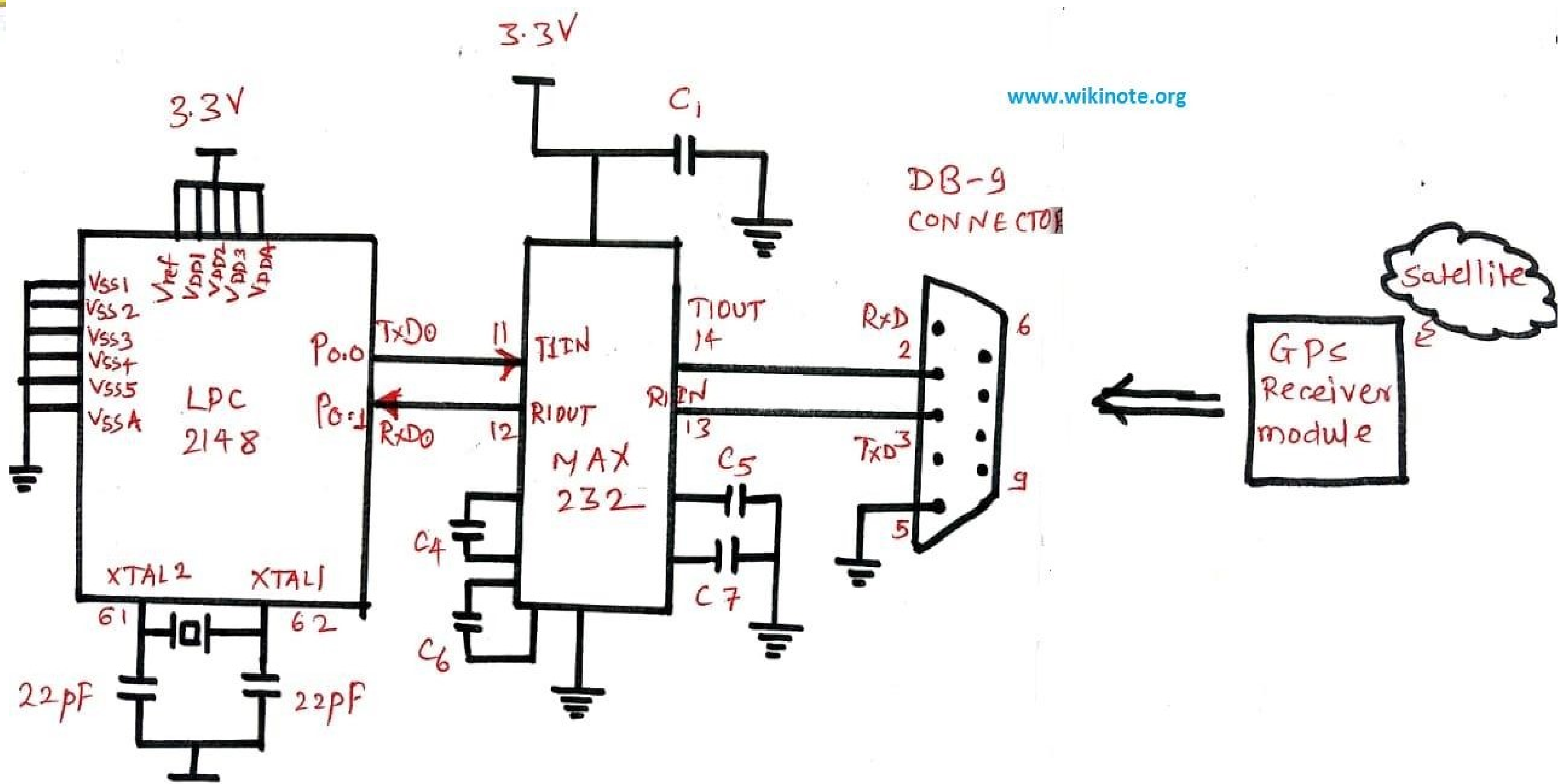
	UART DB-9 Connector	LPC2148 Processor Lines
UART0(P1)	TXD-0	P0.0
	RXD-0	P0.1
UART1(P2)	TXD-1	P0.8
	RXD-1	P0.9

GPS Interfacing with LPC 2148

- The GPS signal is applied to the antenna input of module, and a complete serial data message with position, velocity and time information is presented at the serial interface with NMEA protocol or custom protocol.
- Applications
  - » LBS (Location Based Service)
  - » PND (Portable Navigation Device)
  - » Vehicle navigation system
  - » Mobile phone

GPS Module

GPS Receiver Interfacing with LPC 2148



Pin Assignment with LPC 2148

	UART DB-9 Connector	LPC2148 Processor Lines
UART0(P1)	TXD-0	P0.0
	RXD-0	P0.1
UART1(P2)	TXD-1	P0.8
	RXD-1	P0.9

END